ReRAM ASIC Compute Crossbar

Sddec24-13
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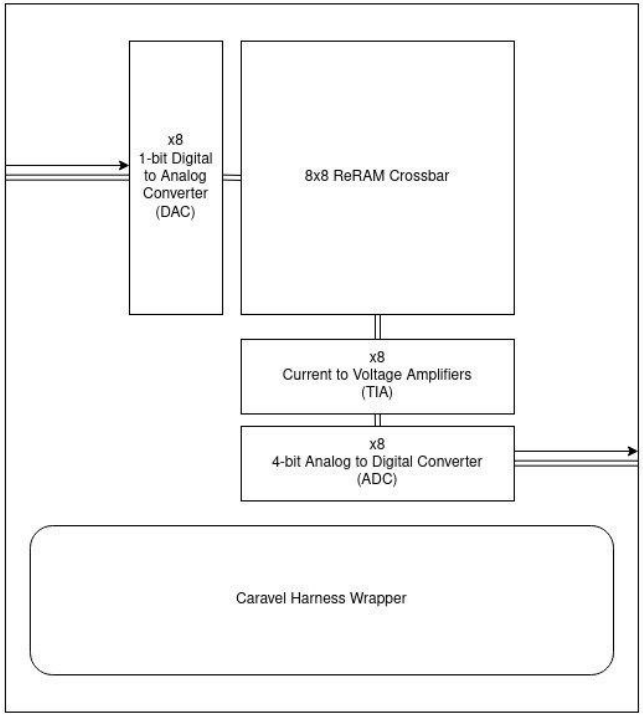
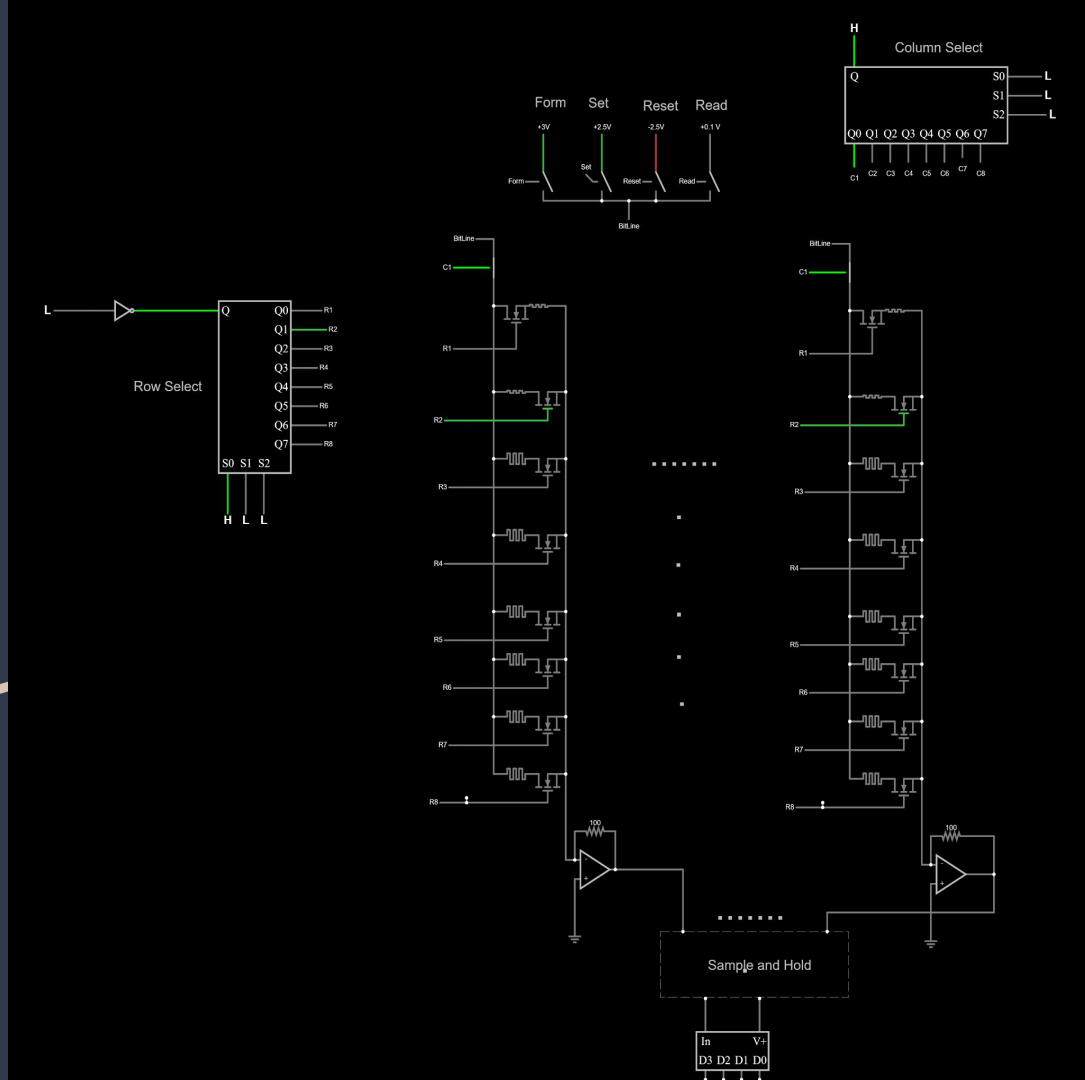
Project Overview

Design a test vehicle for Resistive Random-Access Memory(ReRAM) crossbar for proof of concept

- Utilize open-source design tools
- Submit fabrication application through Efabless shuttle program
- Create bring up plan to test device
- Create documentation for open-source tools for future users



Detailed Design and Visuals

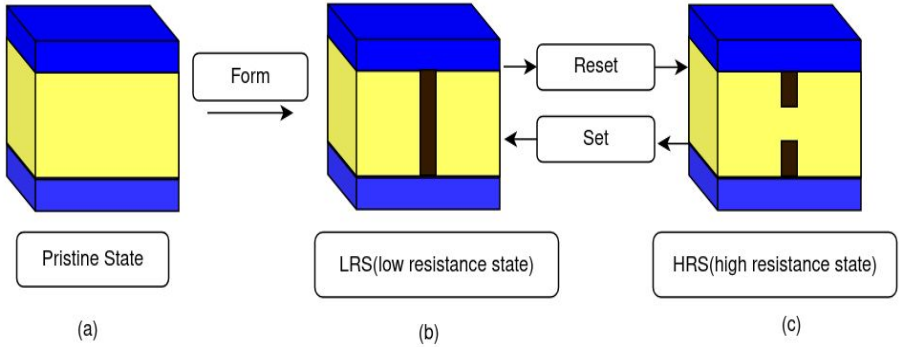


ReRAM cell states

The conductance of a ReRAM cell is dependent on whether the cell is in a LRS(low resistance state) or in a HRS(high resistance state).

- A LRS is viewed as a “digital 1”
- A HRS is viewed as a “digital 0”.

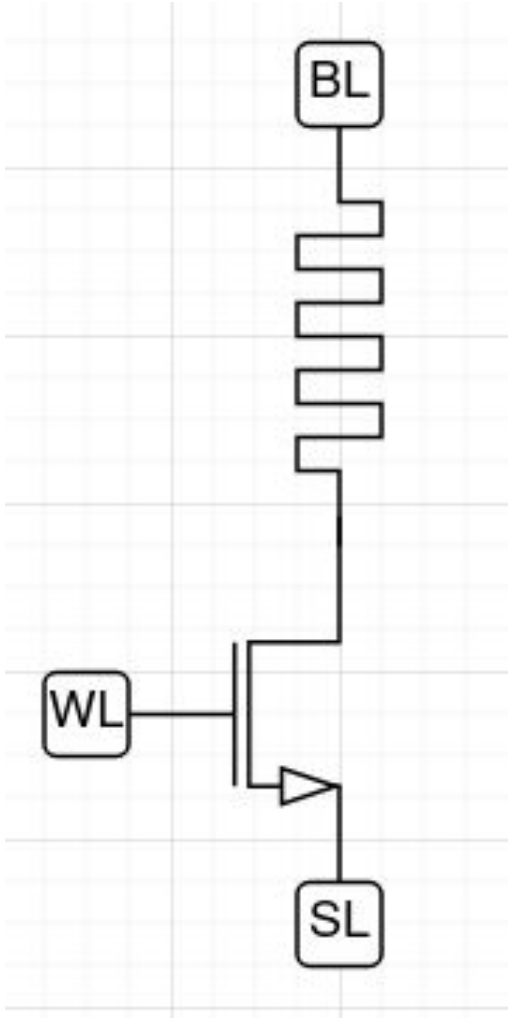
All ReRAM cells start in a pristine state and must be formed into a LRS initially. After the initial form the cell can be set and reset as needed to switch between a digital 1 or 0. This process is illustrated in the image below.



Individual ReRAM cell

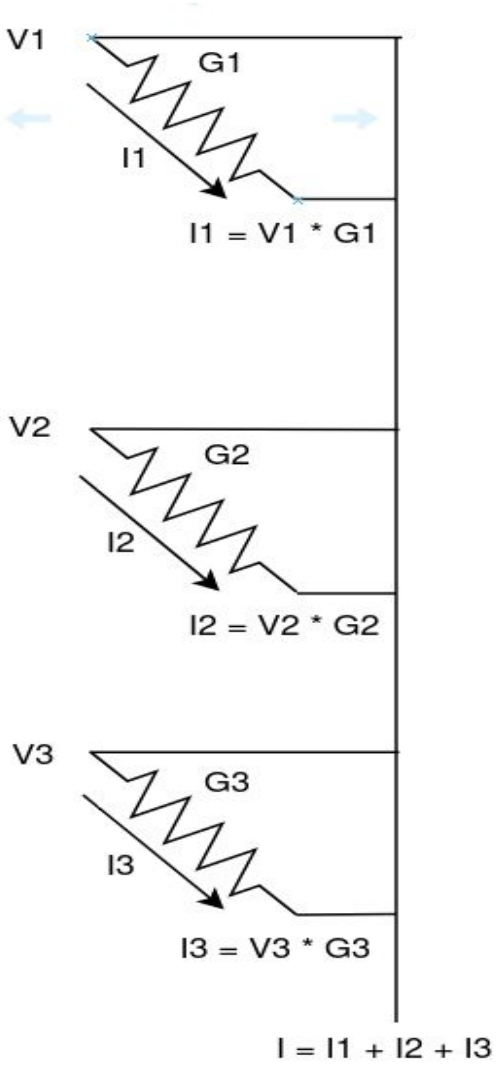
An individual ReRAM cell is shown

- Crossbar will consist of an 8x 8 array of these
- Each contains one resistor and one transistor
  - Referred to as the 1T1R architecture
- Wordline(WL) is connected to a logic analyzer
  - Will determine whether or not the cell is on or off
- Bitline(BL) is connected to the DAC
  - This is where the necessary voltage will be passed into the cell
- SourceLine(SL) is where the current will accumulate to be output

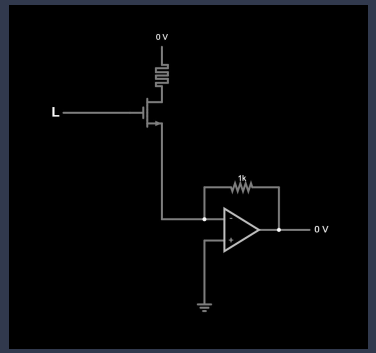


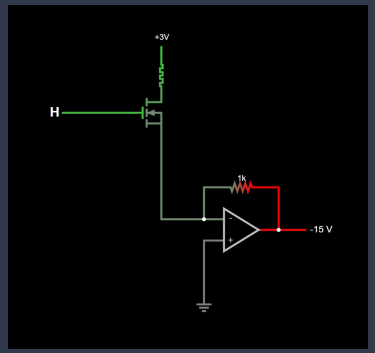
MAC Operation

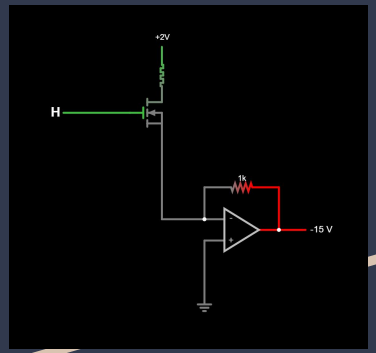
We will use these cells to perform a MAC operation. This operation is illustrated in the image shown where the input voltages, V1,V2 and V3 are multiplied by the conductances, G1,G2, and G3 of the ReRAM and the resulting currents are then summed down along the column to create one output.

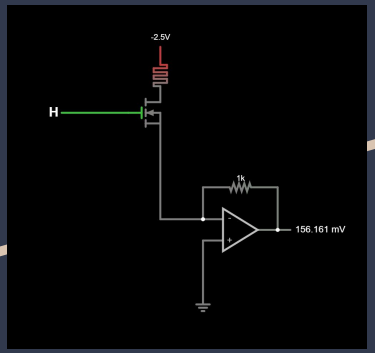


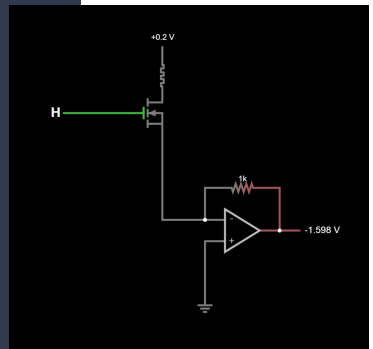
Functionality











1. Initial state
   - High resistance, low conductance
2. Form
   - Power bit ~3.3V and word line ~ 1.8V for 1ms
     - Forms filaments that will be broken and reformed during Sets and Resets
     - After form memristor is in a “high” state
3. Set
   - Power bit ~ 2.5V and word line ~ 1.8V for 1ms
     - Sets the memristor to it’s “high” state
4. Reset
   - Power source ~2.5V and word line ~ 1.8V for 1ms
5. Read
   - Power bit ~0.2 - 0.4 V and word line ~ 2.5 V
     - Allows for reading of memristor state through current analysis but doesn’t change memristor state quickly

Respective states are listed from left to right, top to bottom

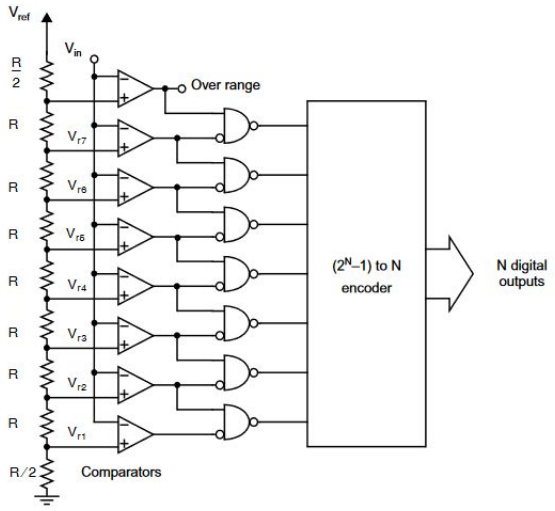


Fig. 17.24 A 3-bit flash A/D converter.